

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT(S): RAUBUCH, MARTIN GROUP ART UNIT: 2183  
APPLN. NO.: 10/531756 EXAMINER: William B. Partridge  
FILED: 04/14/2005  
TITLE: ARRANGEMENT, SYSTEM AND METHOD FOR VECTOR PERMUTATION IN  
SINGLE-INSTRUCTION MULTIPLE-DATA MICROPROCESSORS

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**Certificate of Submission**

I hereby certify that this correspondence is being submitted to the USPTO,  
Alexandria, VA.

- ☐ Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal  
Service with sufficient postage as first class mail.
- ☐ Facsimile transmitted in accordance with C.F.R. § 1.6(d).
- ☒ Submitted electronically via EFS in accordance with "Legal Framework for  
EFS Web".

May 20, 2008

Date of Submission

/Stacie Herrera/

Signature

Stacie Herrera

Printed Name of Person Signing Certificate

**NOTICE OF APPEAL FROM THE EXAMINER TO THE  
BOARD OF PATENT APPEALS AND INTERFERENCES**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SIR:

In accordance with 37 CFR 1.191, applicant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the examiner. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 503079, Freescale Semiconductor, Inc.

Respectfully submitted,  
RAUBUCH, MARTIN  
/David G. Dolezal/

FREESCALE SEMICONDUCTOR, INC.  
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